M5STACK-CORE2

M5STACK

2020

V0.01

1.OUTLINE

M5Stick CORE2 is ESP32 board which based on ESP32-D0WDQ6-V3 chip, contained 2-inch TFT screen. The board is made of PC+ABC.

1.1 Hardware Composition

The hardware of CORE2: ESP32-D0WDQ6-V3 chip, TFT screen, Green LED, Button, GROVE interface, TypeC-to-USB interface, Power Management chip and battery.

ESP32-D0WDQ6-V3 The ESP32 is a dual-core system with two Harvard Architecture Xtensa LX6 CPUs. All embedded memory,external memory and peripherals are located on the data bus and/or the instruction bus of these CPUs.With some minor exceptions (see below), the address mapping of two CPUs is symmetric, meaning that they usethe same addresses to access the same memory. Multiple peripherals in the system can access embeddedmemory via DMA.

TFT Screen is a 2-inch color screen driven ILI9342C with a resolution of 320 x 240. Operating voltage range is 2.6~3.3V, working temperature range is -25~55°C.

Power Management chip is X-Powers's AXP192. The operating voltage range is 2.9V~6.3V and the charging current is 1.4A.

CORE2 equips ESP32 with everything needed for programming, everything needed for operation and development

2. PIN DESCRIPTION

2.1. USB INTERFACE

M5CAMREA Configuration Type-C type USB interface, support USB2.0 standard communication protocol.

2.2. GROVE INTERFACE

4p disposed pitch of 2.0mm M5CAMREA GROVE interfaces, internal wiring and GND, 5V, GPIO32, GPIO33 connected.

3. FUNCTIONAL DESCRIPTION

This chapter describes the ESP32-D0WDQ6-V3 various modules and functions.

3.1. CPU AND MEMORY

Xtensa®single-/dual-core32-bitLX6microprocessor(s), upto600MIPS (200MIPSforESP32-S0WD/ESP32-U4WDH, 400 MIPS for ESP32-D2WD):

- 448 KB ROM
- 520 KB SRAM
- 16 KB SRAM in RTC
- QSPI supports multiple flash/SRAM chips

3.2. STORAGE DESCRIPTION

3.2.1. External Flash and SRAM

ESP32 support multiple external QSPI flash and static random access memory (SRAM), having a hardware-based AES encryption to protect the user programs and data.

- ESP32 access external QSPI Flash and SRAM by caching. Up to 16 MB external Flash code space is mapped into the CPU, supports 8-bit, 16-bit and 32-bit access, and can execute code.
- Up to 8 MB external Flash and SRAM mapped to the CPU data space, support for 8-bit, 16-bit and 32-bit access. Flash supports only read operations, SRAM supports read and write operations.

3.3. CRYSTAL

External 2 MHz~60 MHz crystal oscillator (40 MHz only for Wi-Fi/BT functionality)

3.4. RTC MANAGEMENT AND LOW POWER CONSUMPTION

ESP32 uses advanced power management techniques may be switched between different power saving modes. (See Table 5).

- *Power saving mode*

  - Active Mode: RF chip is operating. Chip may receive and transmit a sounding signal.

  - Modem-sleep mode: CPU can run, the clock may be configured. Wi-Fi / Bluetooth baseband and RF

  - Light-sleep mode: CPU suspended. RTC and memory and peripherals ULP coprocessor operation. Any wake-up event (MAC, host, RTC timer or external interrupt) will wake up the chip.

  - Deep-sleep mode: only the RTC memory and peripherals in a working state. Wi-Fi and Bluetooth connectivity data stored in the RTC. ULP coprocessor can work.

  - Hibernation Mode: 8 MHz oscillator and a built-in coprocessor ULP are disabled. RTC memory to restore the power supply is cut off. Only one RTC clock timer located on the slow clock and some RTC GPIO at work. RTC RTC clock or timer can wake up from the GPIO Hibernation mode.

- *Deep-sleep mode*

  - related sleep mode: power save mode switching between Active, Modem-sleep, Light-sleep mode. CPU, Wi-Fi, Bluetooth, and radio preset time interval to be awakened, to ensure connection Wi-Fi / Bluetooth.

  - Ultra Low-power sensor monitoring methods: the main system is Deep-sleep mode, ULP coprocessor is periodically opened or closed to measure sensor data. The sensor measures data, ULP coprocessor decide whether to wake up the main system.

Functions in different power consumption modes: TABLE 5

Power consumption mode	Active	Modem-sleep	Light-sleep	Deep-sleep	Hibernation
Sleep mode	Associated sleep mode			Ultra low-power Sensor measures data	-
CPU	open	open	pause	close	close
Wi-Fi/Bluetooth Radio	open	open	close	close	close
RTC memory	open	open	open	open	close
ULP coprocessor	open	open	open	open/close	close

4. ELECTRICAL CHARACTERISTICS

4.1. LIMIT PARAMETERS

Table 8: Limiting values

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
I_{output}[1]	Cumulative IO output current	-	1,100	mA
T_{store}	Storage temperature	–40	150	°C

1. V_{IO} to the power supply pad, Refer ESP32 Technical Specification Appendix IO_MUX, as SD_CLK of Power supply for VDD_SDIO.

Press and hold the side power button for two seconds to start the device.Press and hold for more than 6 seconds to turn off the device. Switch to the photo mode through the Home screen, and the avatar that can be obtained through the camera is displayed on the tft screen.The USB cable must be connected when working, and the lithium battery is used for short-term storage to prevent power failure.

FCC Statement:
Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
—Reorient or relocate the receiving antenna.
—Increase the separation between the equipment and receiver.
—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
—Consult the dealer or an experienced radio/TV technician for help.

UIFlow Quick Start

This tutorial applies to M5Core2

Burning tool

Please click the below button to download the corresponding M5Burner firmware burning tool according to your operating system. Unzip and open the application.

中文版

Note: After the installation of MacOS users, please put the application in the Application folder, as shown in the figure below.

Firmware burning

1.Double click to open the Burner burning tool, select the corresponding device type in the left menu, select the firmware version you need, and click the download button to download.

M5Burner
All
Firmware
Images
Map
Apps
Other
Search
Refresh
Refresh Map
Core2
CoreS3
Stick C
Stick C Plus
Stick C Plus2
Stick S3
Stick N4
Stick N2
Cardputer
Cardputer ADV
Tough
Paper
Fire
Gray
Basic
Core
Fire
Gray
Basic
Core
Fire
Gray
Basic
Core